REMARKS

Claims 1-34 are pending in the above-referenced patent application. Claims 1-4, 6-19, 21-27 and 29-34 were rejected. Claims 5, 20 and 28 were objected to as being dependent on rejected base claims, but were deemed allowable if rewritten in independent form including limitations of base claims and any intervening claims.

Claims 1-4, 6-14, 16-19, 21-27, and 29-34 were rejected under 35 USC 112, first paragraph, because the Examiner contents that the specification fails to describe the limitations of selectively activating two of the devices at the same time as recited in claims 1, 9, 17 and 25.

Claims 17-19, 21, 23-27, 29 and 31-32 were rejected under 35 USC 102(e) as being anticipated by USPN 6,697,867 to Chong, Jr. ("Chong"). Claims 9-12 and 15-16 were rejected under 35 USC 103(a) as being unpatentable over Chong in view of USPN 6,725,385 to Chu et al. ("Chu"). Claims 33 and 34 were rejected under 35 USC 103(a) as being unpatentable over Chong in view of USPN 6,772,212 to Lau et al. ("Lau"). Rejection of the claims is respectfully traversed because the references, alone or in combination, do not disclose all of the claimed limitations.

Interview Summary

Applicant wishes to thank the Examiner for the telephonic interview of April 3, 2006, with the undersigned, in which claim rejections under 35 USC 112, and claim rejections involving Chong were discussed.

In regards to rejections under 35 USC 112, Applicant referred the Examiner to specification e.g. page 6, lines 7-10; page 7, lines 5-14; Fig. 1B; page 9, lines 1-7; wherein selectively activating two of the devices at a time is explained. Agreement was reached with the Examiner that rejections under 35 USC 112 should be withdrawn.

In regards to rejections involving Chong, it was discussed that Chong Fig. 1 cannot select any two devices from 21A or 21B, rather Chong must select either 20A and 20B, or select 20C and 20D. It was discussed that Applicant will amend the claims to further clarify that the device controller selectively activates *any* two of the devices a the same time. In this Reply,

Claims 1, 9, 17, 18, 25 and 26 have been amended accordingly to further clarify the claimed limitations. The Examiner indicated that such amendments help further distinguish the claims from Chong.

Rejections under 35 USC 112

Claims 1-4, 6-14, 16-19, 21-27, and 29-34 were rejected under 35 USC 112, first paragraph, because the Examiner contents that the specification fails to describe the limitations of selectively activating two of the devices at the same time as recited in claims 1, 9, 17 and 25. As noted in the above Interview Summary, the specification e.g. on page 6, lines 7-10; page 7, lines 5-14; Fig. 1B; page 9, lines 1-7; etc., amply discloses the steps for selectively activating two of the devices at the same time. As such, the rejections under 35 USC 112 should be withdrawn.

Rejections under 35 USC 102(e)

Rejection of Claims 17-19, 21, 23-27, 29 and 31-32 under 35 USC 102(e) as being anticipated by Chong is respectfully traversed because Chong does not disclose all of the claimed limitations.

Regarding Claims 17 and 25, it is respectfully submitted that Chong fails to disclose that a device controller selectively activates *any* two of the devices at the same time for data communication with the processor over the IDE bus, as claimed. In Chong Fig. 1 cannot select any two devices from 21A or 21B, rather Chong must select either 20A and 20B, or select 20C and 20D. Chong (Fig. 1) can activate only devices in each group 21A (i.e., 20A, 20B) or 21B (i.e., 20C, 20D), but cannot activate at the same time any two devices from among all of the devices 20A, 20B, 20C or 20D, unless they are in the same group. Further, Chong does not disclose utilizing a Cable Select signal, as claimed. Chong uses a chip select (CS) signal, which in the art is different from a Cable Select signal/operation utilized in the present invention. In addition Chong's CS signal is not activating any devices, as claimed. Though Chong mentions master/slave selection, Chong is silent on activating selected devices such that they are active at the same time. In col. 5, lines 13-44 (relied on by the Examiner) Chong mentions selecting

between 21A and 21B in Fig. 1, but no mention of activating any two of the devices at the same time for data communication with the processor over the IDE bus, as claimed.

Chong teaches away from the claimed limitations. In col. 6, lines 54-63, Chong states: "As an example of accessing a particular device, in order to access ATA device 20C, the second value may be stored in control register 26. In response to the second value, signal routing logic 24 produces signals CS0B and CS1B having the same logical values as respective signals CS0 and CS1. ATA devices 20C and 20D are thus selected, and other signals ... may be used to select ATA device 20C from the master/slave pair including ATA devices 20C and 20D." This is in distinct contradiction with the claimed limitations of a device controller selectively activates at most two of the devices at the same time for data communication with the processor over the IDE bus, as claimed, as claimed. For at least these reasons, rejection of Claims 17, 25 and all claimed dependent therefrom should be withdrawn.

Regarding Claims 18, 19, 21, 23, 24, 26, 27, 29, 31 and 32, as dicussed, Chong fails to disclose limitations of base claims 17 and 25. Further, Chong fails to disclose a device controller with features of: identifying *any* one or two devices for data communication with the processor, selecting a first of the identified devices as a master device, if more than one device identified, then selecting the second of the identified devices as a slave device, and activating each selected device, such that a maximum of only two devices are active at the same time, whereby the activated devices can communicate with the processor over the IDE bus, as required by Claims 18 and 26. In col. 6, lines 1-65 and Fig. 1 (relied on by the Examiner) there is no disclosure in Chong of identifying one or two devices, among three or more devices on the IDE bus, for data communication with the processor, as required by Claims 2 and 18. In Chong there are only two ATA devices in either 21A or 21B (Fig. 1), whereby there is no need or disclosure in Chong for a step of identifying among three or more devices on the IDE bus which are active at the same time, as claimed.

In addition, Chong (Fig. 1) can activate only devices in each group 21A (i.e., 20A, 20B) or 21B (i.e., 20C, 20D), but cannot activate at the same time *any* two devices from among all of the devices 20A, 20B, 20C or 20D, unless they are in the same group. Further, Chong does not

disclose utilizing a Cable Select signal, as claimed. Chong uses a chip select (CS) signal, which in the art is different from a Cable Select signal/operation utilized in the present invention. In addition Chong's CS signal is not activating any devices, as claimed.

Further, there is no need or disclosure in Chong for the decision step: if more than one device is identified, then selecting the second of the identified devices as a slave device, as required by Claims 2 and 18. Because as discussed there is no identification step in Chong, there is no need or disclosure for checking if more than one device has been identified. And, as such, there is no need or disclosure for *selecting* a second identified device, among three or more devices on the same IDE bus, as a slave. For that matter, there is no disclosure in Chong of selecting a first identified device among three or more devices on the IDE bus, as a master.

Further, Chong does not disclose: activating each selected device, such that a maximum of only two devices among said three or more devices are active at the same time, as required by Claims 2 and 18. Though Chong mentions master/slave selection, Chong is silent on activating selected devices such that they are active at the same time. This allows the activated devices to communicate with the processor over the IDE bus, as required by Claims 18 ands 26. Chong teaches away from the claimed limitations. In col. 6, lines 54-63 (relied on by the Examiner) Chong states: "As an example of accessing a particular device, in order to access ATA device 20C, the second value may be stored in control register 26. In response to the second value, signal routing logic 24 produces signals CS0B and CS1B having the same logical values as respective signals CS0 and CS1. ATA devices 20C and 20D are thus selected, and other signals ... may be used to select ATA device 20C from the master/slave pair including ATA devices 20C and 20D." This is in distinct contradiction with the claimed limitations of: activating each selected device, such that a maximum of only two devices among said three or more devices are active at the same time, as required by Claims 18 and 26. For at least theses reasons, rejection of Claims 18 and 26 should be withdrawn.

Regarding Claims 19 and 27, Chong does not disclose that a device controller is configured to activate a maximum of two of said three or more devices connected to the IDE bus at the same time, and to deactivate the remaining of said three or more devices, as claimed. In col.

6, lines 54-63 (relied on by the Examiner) Chong states: "As an example of accessing a particular device, in order to access ATA device 20C, the second value may be stored in control register 26. In response to the second value, signal routing logic 24 produces signals CS0B and CS1B having the same logical values as respective signals CS0 and CS1. ATA devices 20C and 20D are thus selected, and other signals ... may be used to select ATA device 20C from the master/slave pair including ATA devices 20C and 20D." This is in distinct contradiction with the claimed limitations of activating two of said three or more devices connected to the IDE bus at the same time. In addition, Chong (Fig. 1) can activate only devices in each group 21A (i.e., 20A, 20B) or 21B (i.e., 20C, 20D), but cannot activate at the same time any two devices from among all of the devices 20A, 20B, 20C or 20D, unless they are in the same group. Further, Chong does not disclose utilizing a Cable Select signal, as claimed. Chong uses a chip select (CS) signal, which in the art is different from a Cable Select signal/operation utilized in the present invention. In addition Chong's CS signal is not activating any devices, as claimed. For at least these reasons, rejection of Claims 19 and 27 should be withdrawn.

Regarding Claims 23 and 31, Chong, col. 1, lines 13-25 and col. 5, lines 13-44 (relied on by the Examiner) does not disclose an interface controller connected to said devices via the IDE bus, wherein the interface controller manages information flow between the processor and said devices over the IDE bus, as required by Claims 23 and 31. In col. 1, lines 13-25, Chong simply mention various prior art ATA devices, which have nothing to do with the claimed limitation. Further, in col. 5, lines 13-44, Chong describes various selection signals for selecting a single ATA device in 21A or 21B (Fig. 1). There is no mention there on an interface controller that manages information flow between the processor and said devices over the IDE bus, as claimed. There is no interface device discussed or suggested in Chong. The Examiner has not pointed to a disclosure of such limitations in Chong. Further, because as in Stryker, Chong activates a single ATA device, there is no need for a specialized interface controller as claimed, to manage information flow between the processor and devices over the IDE bus which can be active at the same time. In addition, Chong (Fig. 1) can activate only devices in each group 21A (i.e., 20A, 20B) or 21B (i.e., 20C, 20D), but cannot activate at the same time any two devices from

among all of the devices 20A, 20B, 20C or 20D, unless they are in the same group. Further, Chong does not disclose utilizing a Cable Select signal, as claimed. Chong uses a chip select (CS) signal, which in the art is different from a Cable Select signal/operation utilized in the present invention. In addition Chong's CS signal is not activating any devices, as claimed. For at least these reasons, rejection of Claims 23 and 31 should be withdrawn.

Rejection of Claims 9-12 and 15-16 under 35 USC 103(a)

Rejection of Claims 9-12 and 15-16 under 35 USC 103(a) as being unpatentable over Chong in view of Chu is respectfully traversed because the references, alone or in combination, do not disclose all of the claimed limitations.

As per Claim 9, in col. 6, lines 1-65 and Fig. 1 (relied on by the Examiner), or elsewhere in Chong, there is no disclosure of identifying *any* one or *any* two devices, among three or more devices on the IDE bus, for data communication with the processor, as claimed. In Chong there are only two ATA devices in either 21A or 21B (Fig. 1), whereby there is no need or disclosure in Chong for a step of identifying among three or more devices on the IDE bus which are active at the same time, as claimed. Further, there is no need or disclosure in Chong for the decision step: if more than one device is identified, then selecting the second of the identified devices as a slave device, as required by Claims 2 and 18. Because as discussed there is no identification step in Chong, there is no need or disclosure for checking if more than one device has been identified. And, as such, there is no need or disclosure for *selecting* a second identified device, among three or more devices on the same IDE bus, as a slave. For that matter, there is no disclosure in Chong of selecting a first identified device among three or more devices on the IDE bus, as a master. In addition, Chong (Fig. 1) can activate only devices in each group 21A (i.e., 20A, 20B) or 21B (i.e., 20C, 20D), but cannot activate at the same time any two devices from among all of the devices 20A, 20B, 20C or 20D, unless they are in the same group. Further, Chong does not disclose utilizing a Cable Select signal, as claimed. Chong uses a chip select (CS) signal, which in the art is different from a Cable Select signal/operation utilized in the present invention. In addition Chong's CS signal is not activating any devices, as claimed.

Further, Chong does not disclose: activating each selected device, such that *any* two devices among said three or more devices are active at the same time, as claimed. Though Chong mentions master/slave selection, Chong is silent on activating selected devices such that they are active at the same time. This allows the activated devices to communicate with the processor over the IDE bus, as claimed. Indeed, Chong teaches away from the claimed limitations. In col. 6, lines 54-63 (relied on by the Examiner) Chong states: "*As an example of accessing a particular device, in order to access ATA device 20C*, the second value may be stored in control register 26. In response to the second value, signal routing logic 24 produces signals CS0B and CS1B having the same logical values as respective signals CS0 and CS1. ATA devices 20C and 20D are thus selected, and *other signals ... may be used to select ATA device 20C from the master/slave pair including ATA devices 20C and 20D.*" (emphasis added). This is in distinct contradiction with the claimed limitations of: activating each selected device, such that a maximum of only two devices among said three or more devices are active at the same time, as required by Claim 9.

Further, as the Examiner also states, Chong does not disclose a method for communicating data between a processor and three or more devices over an IDE bus by first deactivating all the devices, as required by Claim 1. However, the Examiner interprets Chong, col. 2, lines 25-34, and Chu to disclose such a limitation. These interpretations of Chong and Chu are respectfully traversed. In col. 2, lines 25-34 (relied on by the Examiner), Chong simply mentions: "The signal routing logic receives an access signal from the host system and routes the access signal to the group access signal for the group of peripheral devices selected by the value stored in the control register. The group access signal for each of the remaining groups of peripheral devices is deasserted so that the groups of peripheral devices not selected by the value stored in the control register are not accessed (i.e., do not respond to accesses from the host system)." In this passage, or elsewhere in Chong, there is not single word about activating or deactivating any devices. Nor is there any disclosure or need in Chong about deactivating any of the devices since Chong uses device selection for accessing a single device (as discussed above). The Examiner's interpretation of Chong is respectfully traversed.

Further, Chu has nothing to do with the present invention. Chu is directed to a device connected to an interface has operational logic and power control logic. The device further has multiple power modes, including a first mode and a second, lower power mode. In the first mode, the operational logic is coupled to the interface, and is able to communicate over the interface. In the second mode, the power control logic is coupled to the interface, and the operational logic is decoupled, and substantially powered down. This provides a low interface power mode. In this mode, the power control logic monitors the interface for command activity. The power control logic returns the device to the first mode when the device must be in the first mode to process or reply to the command. The power control logic thus provides for the restoration of function from a low interface power mode without the need for a special "wake-up" command, thereby making the low interface power mode transparent to the host (Abstract). There is no mention or suggestion in Chu of connecting three or more IDE devices to an IDE bus, to extend capability of an IDE bus according to the present invention. Chu is entirely concerned with power consumption and a power controller to control interface power consumption of a device so that the device power consumption is reduced from that in low-power modes of the devices (col. 1, lines 54-57). Indeed, Chu is non-analogous art.

Further, Chu, col. 1, lines 13-53, col. 2, lines 12-30, col. 3, lines 45-67 does not disclose deactivating all of the devices on an IDE bus. In col. 1, lines 13-19, Chu mentions various power modes of HDDs, wherein in every mode at least a part of the HDD is powered. This has nothing to do with the claimed limitations of deactivating all of the devices. Chu, col. 1, lines 13-19, states: "Hard Disk Drives (HDDs) have multiple power modes that trade-off energy consumption for response time. Accordingly, a relatively short response time has an associated relatively higher energy consumption because a greater proportion of the HDD is powered up and active. Typical power modes for an HDD include Active, Idle, Standby and Sleep modes. Other mobile computer peripheral devices, such as a microprocessor (μP) and a liquid crystal display (LCD), provide power modes that are analogous to HDD power modes." As such, unlike the claimed limitations, according to Chu, in various power modes at least a part of the device is

powered. There is no disclosure in Chu of all devices on an IDE bus being deactivates, as claimed.

It is well settled that in order for a modification or combination of the prior art to be valid, the prior art itself must suggest the modification or combination. There is no motivation or suggestion, motivation or need in Chong for saving power as the Examiner suggests. Chu is only concerned about reducing power consumption, and in no way related to a method for communicating data between a processor and three or more devices over an IDE bus, as claimed. There is no motivation or suggestion in either reference to combine them. Even if Chong is modified according to Chu as the Examiner suggests, the resulting system is one in which the IDE devices may operate at lower power levels, but will not be deactivated. At any rate, a deactivation of all of the IDE devices in Chong would be disruptive to Chong's selecting circuit. Further, even if all of the devices in Chong are deactivated, there is no disclosure anywhere in Chong that such a deactivation allows Chong to select more than one device at a time. Accordingly, any modification of Chong using Chu as suggested by the Examiner, still does not disclose the claimed limitations. There is no disclosure in the references, alone or in combination, of deactivating all of the devices, selecting one or more devices, and activating at most two selected devices at the same time to communication with a processor. Controlling power consumption of devices has nothing to do with the claimed limitations of deactivating all of the devices, and reactivating selected devices as part of a method for communicating data between a processor and three or more devices over an IDE bus, as claimed. For at least these reasons, rejection of Claim 9 and all claims dependent therefrom should be withdrawn.

As per Claim 10, for at least the reasons provided in relation to Claim 9, the references alone or in combination do not disclose the step of deactivating all of the devices after communication between the processor and each activated device. As per Claim 11, for at least the reasons provided in relation to Claims 9 and 10, the references alone or in combination do not disclose repeating the process of deactivating all of the devices, selecting any or two devices, and activating at most two selected devices at the same time to communication with a processor. As per Claim 15, for at least the reasons provided in relation to Claim 9, despite the Examiner's

assertion, the references alone or in combination do not disclose powering off all devices, and then powering on selected devices. In Chu, col. 6, lines 21-65 (relied on by the Examiner) there is not a single word about powering off all devices. Nor is there any mention of powering on selected devices. If the Examiner believes otherwise, Applicant respectfully requests a specific reference or quotation in Chu, rather than broad reference to lengthy sections of Chu that have nothing to do with the claimed limitations. Further, Chu does not power devices on and off, rather Chu controls how much power is supplied to the devices without powering them off. For at least these reasons, rejection of Claim 15 should be with withdrawn.

Rejection of Claims 33 and 34 under 35 USC 103(a)

Rejection of Claims 33 and 34 under 35 USC 103(a) as being unpatentable over Chong in view of Lau is respectfully traversed because the references, alone or in combination, do not disclose all of the claimed limitations.

As discussed, Chong does not disclose all of the limitations of Claim 25. Further, Lau is non-analogous art. Lau, is directed to an audio/visual server that can be used to store and play audio/visual data. A removable hard disk (or other media) is connected to a dock that is in communication with a computer. While the removable hard disk is connected to the dock, audio/visual data can be transferred from the computer to the hard disk. After the hard disk is removed from the dock and connected to the audio/visual server, the server can access and play the audio/visual data. (Abstract). In col. 5, lines 26-47, Lau discusses FIG. 3 as a schematic of the internal components of docking station 122. Wire 142 is connected to switch 150. Switch 150 is a mechanical switch that is triggered when disk cartridge 120 is completely and properly inserted into opening 140. Switch 150 is connected to IDE controller 152 and USB to IDE interface 154. When switch 150 is triggered (disk cartridge 120 is inserted in docking station 122), power from wire 142 is provided to IDE connector 152 and USB to IDE interface 154. Wire 144 connects docking station 122 to a USB port of computer 124.

However, in Lau, IDE connector 152 in Lau is not an IDE bus, as claimed. The IDE connector is simply for connecting one IDE device to element 154, and cannot server as an

IDE bus. Further, the USB-to-IDE interface 154 only connects on device (disk drive connected to IDE connector 152) to a USB post of a computer 124 via wire 144. Lau, does not disclose that the interface 154 is a USB-to-IDE controller connected between an IDE bus and the processor, such that multiple storage devices are connected to the USB-to-IDE controller via the IDE bus, as claimed. Nor does Lau mention that the interface 154 can connect more than one IDE device to the computer 124. By contrast, according to Claims 33 and 34, more than one device communicates with the processor via the USB-to-IDE controller over the IDE bus.

There is no suggestion or motivation in the references themselves to combine them as the Examiner suggests. One of ordinary skill in the would not look to Chong or Lau to solve the problems addressed by the present invention. Chong (Fig. 1) can activate only devices in each group 21A (i.e., 20A, 20B) or 21B (i.e., 20C, 20D), but cannot activate at the same time any two devices from among all of the devices 20A, 20B, 20C or 20D, unless they are in the same group. Further, Chong does not disclose utilizing a Cable Select signal, as claimed. Chong uses a chip select (CS) signal, which in the art is different from a Cable Select signal/operation utilized in the present invention. In addition Chong's CS signal is not *activating* any devices, as claimed. Further, Chong does not disclose a USB to IDE controller connected between the IDE bus and the processor, as claimed. In addition, Lau does not provide a does not teach that the interface 154 is a USB-to-IDE controller connected between an IDE bus and the processor, such that multiple storage devices are connected to the USB-to-IDE controller via the IDE bus, as claimed. Nor does Lau teach that the interface 154 can connect more than one IDE device to the computer 124. By contrast, according to Claims 33 and 34, more than one device communicates with the processor via the USB-to-IDE controller over the IDE bus. The Examiner is using hindsight based on teachings of the claimed invention to combine Chong and Lau.

Further, Chong or Lau, alone or in combination, do no disclose a USB controller connected to the processor, wherein the USB-to-IDE controller is connected between the IDE bus and the USB controller, such that the device controller selectively activates the devices for data communication with the processor via the USB controller and the USB-to-IDE controller over the IDE bus (Claim 34). There is no arrangement in the references of devices that communicate with

a processor a USB controller and a USB-to-IDE controller over the IDE bus, as claimed. For at least these reasons, rejection of Claims 33 and 34 should be withdrawn.

CONCLUSION

For the foregoing, and other, reasons Applicants believe that the rejected claims should be allowed. Reconsideration and allowance of the rejected claims are respectfully requested. Please continue to direct all communications regarding the above-referenced patent application to the principal agent of record.

Respectfully Submitted,

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CERTIFICATE OF MAILING

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